

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

DATE MAILED: 06/15/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,529	04/01/2004	Scott D. Brandenburg	DP-311272	1574
75	90 06/15/2006		EXAM	INER
DOUGLAS D. FEKETE			CAO, PHAT X	
DELPHI TECH	NOLOGIES, INC.			
Legal Staff, Mail Code: 480-410-202			ART UNIT	PAPER NUMBER
P.O. Box 5052			2814	
Trov MI 4800	7-5052			

Please find below and/or attached an Office communication concerning this application or proceeding.

			P
	Application No.	Applicant(s)	-
	10/815,529	BRANDENBURG ET AI	L.
Office Action Summary	Examiner	Art Unit	
	Phat X. Cao	2814	
The MAILING DATE of this communication ap	opears on the cover sheet	with the correspondence address	s
Period for Reply		MONTHON OF THETH (60) F	1)/0
A SHORTENED STATUTORY PERIOD FOR REP WHICHEVER IS LONGER, FROM THE MAILING I - Extensions of time may be available under the provisions of 37 CFR 1 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory perior Failure to reply within the set or extended period for reply will, by statu Any reply received by the Office later than three months after the mail earned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUN .136(a). In no event, however, may d will apply and will expire SIX (6) M tte, cause the application to become	NICATION. a reply be timely filed ONTHS from the mailing date of this commun ABANDONED (35 U.S.C. § 133).	
Status			
1) Responsive to communication(s) filed on 23	March 2006.		
	is action is non-final.		
3) Since this application is in condition for allow		atters, prosecution as to the mer	rits is
closed in accordance with the practice under	Ex parte Quayle, 1935 C	.D. 11, 453 O.G. 213.	
Disposition of Claims			
4)⊠ Claim(s) <u>1 and 3-9</u> is/are pending in the appl	ication.		
4a) Of the above claim(s) is/are withdr	awn from consideration.		
5) Claim(s) is/are allowed.			
6)⊠ Claim(s) <u>1, 3-9</u> is/are rejected.			
7) Claim(s) is/are objected to.			
8) Claim(s) are subject to restriction and	or election requirement.		
Application Papers			
9)☐ The specification is objected to by the Examir	ner.		
10) ☐ The drawing(s) filed on is/are: a) ☐ ac	ccepted or b) objected	o by the Examiner.	
Applicant may not request that any objection to th	e drawing(s) be held in abey	ance. See 37 CFR 1.85(a).	
Replacement drawing sheet(s) including the corre			
11)☐ The oath or declaration is objected to by the B	Examiner. Note the attach	ed Office Action or form PTO-19	52.
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreig	gn priority under 35 U.S.C	. § 119(a)-(d) or (f).	
a) ☐ All b) ☐ Some * c) ☐ None of:			
1. Certified copies of the priority docume	nts have been received.		
2. Certified copies of the priority docume	nts have been received in	Application No	
Copies of the certified copies of the pri	iority documents have be	en received in this National Stag	je
application from the International Bure	au (PCT Rule 17.2(a)).		
* See the attached detailed Office action for a list	st of the certified copies n	ot received.	
Attachment(s)			
1) Notice of References Cited (PTO-892)	4) T Intervie	w Summary (PTO-413)	
2) D Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper N	lo(s)/Mail Date	\
 Information Disclosure Statement(s) (PTO-1449 or PTO/SB/0 Paper No(s)/Mail Date 	(8) 5) ☐ Notice 6 6) ☐ Other: _	of Informal Patent Application (PTO-152))

Art Unit: 2814

DETAILED ACTION

1. The cancellation of claims 1, 3, 9 and 10-19 in Paper filed on 3/23/06 is acknowledged.

Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1, 3, 5-6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al (US. 6,571,466) in view of Carney et al (US. 5,895,229).

Regarding claims 1, 5 and 9, Glenn (Fig. 4) discloses a microelectronic assembly comprising: a substrate 102 formed of a glass transparent material (column 8, lines 44-47 and lines 55-57), an integrated circuit die 104 having an active face facing the substrate 102 and a rear face 104U opposite the active face, the active face including a central region and a perimeter region about the central region, a plurality of bump interconnections 1 12 attaching the integrated circuit die 104 to the substrate 102 such that the active face is spaced apart from the substrate 102 by a gap 118, an epoxy encapsulant 116 (column 10, lines 47-48) about the integrated circuit die 104 on the substrate 102, overlying the rear face 104U of the die 104 (also see column 10, lines 31-35), and extending within the gap 1 18 to encapsulate the bump interconnections 1 12, and an optical window 120 defined by the encapsulant 116 within the gap 120 between the central region 1 18 and the substrate 102.

Art Unit: 2814

ţ

1

Glenn does not disclose that the epoxy encapsulant 116 is a polymeric encapsulant having sides perpendicular to the substrate.

However, Carney (Fig. 6) teaches the forming of an epoxy encapsulant 238 being a polymeric encapsulant (column 5, lines 9-12 and column 3, lines 54-61) and having sides perpendicular to the substrate 248. The polymeric encapsulant 238 is formed over and between the chip 212 and the glass substrate 248 for providing enhanced reliability to the assembly. Accordingly, it would have been obvious to form the epoxy encapsulant 116 of Glenn with an epoxy polymeric material because as taught by Carney, such encapsulant polymeric material is well known and commonly used for providing enhanced reliability to the assembly by distributing the stresses from the solder bumps and also by encapsulating the solder bump interconnections so that they are not subject to environment degradation (column 1, lines 44-48).

Regarding claim 3, Glenn (Fig. 4) further discloses that the central region of the die 104 comprises an optical feature 106 adapted for detecting/emitting optical signals through the substrate 102 (column 8, lines 44-47).

Regarding claim 8, Glenn (Fig. 4) further discloses that the bump interconnections 1 12 are bonded to the die 104 at the perimeter region and to the substrate 102.

Regarding claim 6, Carney further teaches that the polymeric encapsulant 238 (Fig. 6) or 36 (Fig. 2) is composed of an epoxy polymer and comprises an inorganic particular filler of silica or alumina (column 3, lines 54-57).

Art Unit: 2814

ŗ

4

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al and Carney et al as applied to claim 1 above, and further in view of Gonzalez et al (US. 2003/0080437).

As discussed in details above, the combination of Glenn and Carney substantially reads on the above claim. Carney (Fig. 6) further discloses that the encapsulant 238 is a polymeric filled with inorganic filler of silica or alumina (column 3, lines 54-57).

Carney does not disclose the polymeric encapsulant 238 has a thermal expansion coefficient (CTE) in a range as claimed.

However, Gonzalez (Fig. 6) teaches the forming of inorganic filler encapsulant 1 16 (par. (OO38J) between the chip 130 and the FR-4 glass substrate 110 (par. (0040)). The inorganic filler encapsulant 116 has lower CTE and has relatively closer CTE match to the chip 130 and the substrate 1 10 by adding a suitable amount of inorganic filler in a range of 0% to 80% by weight (par. (0039) and par. (0040)). Accordingly, it would have been obvious to adjust the thermal expansion coefficient (CTE) of the filler encapsulant 238 in a range as claimed for providing the closer CTE match between the chip and the substrate because the CTE of the filler encapsulant can be controlled depending upon the CTE of the glass substrate and depending upon the amount of filler (0% to 80%) added to the encapsulant, as taught by Gonzalez (par. (0040)).

Art Unit: 2814

4

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al and Carney et al as applied to claim 1 above, and further in view of Chason et al (US. 6,800,946).

Neither Glenn nor Carney discloses that the polymeric encapsulant is opaque.

However, Chason (Fig. 2) teaches an opto-electronic assembly having the polymeric encapsulant 240 disposed between the optical chip 210 and the substrate 130, the polymeric encapsulant 240 is transparent, partially transparent, or opaque over the wavelengths of interest 9column 8, lines 24-38). Accordingly, it would have been obvious to form the polymeric encapsulant of the above combination device being transparent, partially transparent, or opaque depending upon the desired wavelengths for the optical device, as taught by Chason.

6. Claims 1, 3, 5-6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carney et al (US. 5,895,229) in view of Glenn et al (US. 6,571,466).

Regarding claims 1, 5 and 9, Carney (Fig. 6) discloses a microelectronic assembly comprising: a glass substrate 248 or 14 (column 2, lines 56-60), an integrated circuit die 212 having an active face facing the substrate 248 and a rear face opposite the active face, the active face including a central region and a perimeter region about the central region, a plurality of bump interconnections 216 attaching the integrated circuit die 212 to the substrate 248 such that the active face is spaced apart from the substrate 248 by a gap, a polymeric encapsulant 238 formed of a molded body (column 5, lines 9-11 and column 3, lines 54-57) about the integrated circuit die 212 on the substrate 248 and overlying the rear surface, the polymeric encapsulant 238 having

Art Unit: 2814

٤

Ó

A-4 | |----- 004.4

sides perpendicular to the substrate 248 and extending within the gap to encapsulate the bump interconnections 216.

Carney does not disclose an optical window defined within the gap.

However, Glenn (Fig. 4) teaches an image sensor package having an optical window 106 defined by the encapsulant 116 within the gap 120 between the central region of an optical chip 104 and a glass transparent substrate 102 (column 8, lines 44-47 and lines 55-57). Accordingly, it would have been obvious to modify the microelectronic assembly of Carney by forming an optical window within the gap between the central region and the substrate in order to form an image sensor package, as taught by Glenn (column 5, lines 32-34).

Regarding claim 3, Glenn (Fig. 4) further teaches that the central region of the die 104 comprises an optical feature 106 adapted for detecting/emitting optical signals through the substrate 102 (column 8, lines 44-47).

Regarding claim 8, Carney (Fig. 6) further discloses that the bump interconnections 216 are bonded to the die 212 at the perimeter region and to the substrate 248.

Regarding claim 6, Carney further discloses that the polymeric encapsulant 238 (Fig. 6) or 36 (Fig. 2) is composed of an epoxy polymer and comprises an inorganic particular filler of silica or alumina (column 3, lines 54-57).

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carney et al and Glenn et al as applied to claim 1 above, and further in view of Gonzalez et al (US. 2003/0080437).

Art Unit: 2814

1

As discussed in details above, the combination of Glenn and Carney substantially reads on the above claim. Carney (Fig. 6) further discloses that the encapsulant 238 is a polymeric filled with inorganic filler of silica or alumina (column 3, lines 54-57).

Carney does not disclose the polymeric encapsulant 238 has a thermal expansion coefficient (CTE) in a range as claimed.

However, Gonzalez (Fig. 6) teaches the forming of inorganic filler encapsulant 1 16 (par. (OO38J) between the chip 130 and the FR-4 glass substrate 110 (par. (0040)). The inorganic filler encapsulant 116 has lower CTE and has relatively closer CTE match to the chip 130 and the substrate 1 10 by adding a suitable amount of inorganic filler in a range of 0% to 80% by weight (par. (0039) and par. (0040)). Accordingly, it would have been obvious to adjust the thermal expansion coefficient (CTE) of the filler encapsulant 238 in a range as claimed for providing the closer CTE match between the chip and the substrate because the CTE of the filler encapsulant can be controlled depending upon the CTE of the glass substrate and depending upon the amount of filler (0% to 80%) added to the encapsulant, as taught by Gonzalez (par. (0040)).

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carney et al and Glenn et al as applied to claim 1 above, and further in view of Chason et al (US. 6,800,946).

Neither Glenn nor Carney discloses that the polymeric encapsulant is opaque.

Art Unit: 2814

١

However, Chason (Fig. 2) teaches an opto-electronic assembly having the polymeric encapsulant 240 disposed between the optical chip 210 and the substrate 130, the polymeric encapsulant 240 is transparent, partially transparent, or opaque over the wavelengths of interest 9column 8, lines 24-38). Accordingly, it would have been obvious to form the polymeric encapsulant of the above combination device being transparent, partially transparent, or opaque depending upon the desired wavelengths for the optical device, as taught by Chason.

Page 8

Response to Arguments

- 9. In response to Applicant's argument that Glenn does not suggest the molded polymeric encapsulant having sides perpendicular to the substrate as amended, the new reference issued to Carney et al is applied in the new ground of rejections to show the known feature of forming molded polymeric encapsulant.
- 10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC

June 9, 2006

PHAT X. CAO

Page 9